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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,113	07/11/2003	Rajeev Joshi	11948.21	8697
27966	7590	09/01/2004	EXAMINER	
KENNETH E. HORTON KIRTON & MCCONKLE 60 EAST SOUTH TEMPLE SUITE 1800 SALT LAKE CITY, UT 84111			ZARNEKE, DAVID A	
		ART UNIT	PAPER NUMBER	
			2829	
DATE MAILED: 09/01/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,113	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zameke	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02 July 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-33 is/are pending in the application.
 4a) Of the above claim(s) 1-19 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 20-33 is/are rejected.
 7) Claim(s) 24, 28 and 30 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 11 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 10/295281.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>11/04/03; 1/23/04; 5/10/04</u>	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group II, claims 20-33, in the reply filed on 7/2/04 is acknowledged. The traversal has been found to be persuasive.

Applicant was correct in stating that the restriction requirement was incomplete. The claims were mistakenly not shown to be independent from each other.

Therefore, the requirement has been removed. A new restriction requirement will now be provided.

Claims 1-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected group, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7/2/04.

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-19, drawn to a package, classified in class 257, subclass 700.
- II. Claims 20-3, drawn to a method of making the package, classified in class 438, subclass 612.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process

(MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process. For example, instead of forming without using a high temperature curing process, one could use a high temperature curing process.

This reasoning was provided before and was traversed by applicant. It was stated that the independent claims did not require the limitation and therefore was incorrect.

The examiner notes that the reasoning need not be provided in the independent claim. The reasoning can be provided from any of the dependent claims too.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 recites the limitation "RDL pattern" on line 5. There is insufficient antecedent basis for this limitation in the claim.

For examination purposes the examiner assumes that the metal layer and the RDL pattern refer to the same element.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20, 22 and 23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Higgins, III, US Patent 6,294,405 (hereafter Higgins).

Higgins (Figure 1) teaches a method of making a wafer-level chip scale package, comprising:

providing a chip pad (14) over a substrate (11);

providing a re-distributed line (RDL) pattern (16) on the chip pad;

providing an insulating layer (18) covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material (2, 65+); and

providing a stud bump (20) on the portion of the RDL pattern not covered by the insulating layer.

Regarding claim 22, Higgins teaches the insulating layer comprises SiN (2, 65+).

With respect to claim 23, Higgins does not teach using a UBM between the chip pad and the RDL.

Claims 24, and 26-28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Higgins, III, US Patent 6,294,405 (hereafter Higgins).

Higgins (Figure 1) teaches a method of making a wafer-level chip scale package, comprising:

providing a substrate (11) with a passivation layer (12) on a portion thereof;

forming a chip pad (14) on a portion of the substrate not containing the passivation layer;

forming a metal layer (16) on the chip pad and a portion of the passivation layer;

forming an insulating layer (18) on a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material (2, 65+); and

forming a stud bump (20) on the portion of the RDL pattern not covered by the insulating layer.

Regarding claim 26, Higgins teaches the insulating layer comprises SiN (2, 65+).

With respect to claims 27, while Higgins fails to expressly state that the insulating layer is formed without using a high temperature curing process, SiN inherently uses a low temperature curing process.

As to claim 28, Higgins does not teach using a UBM between the chip pad and the RDL.

Claim 32 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Higgins, III, US Patent 6,294,405 (hereafter Higgins).

Higgins (Figure 1) teaches a method of making a package semiconductor device, comprising:

- providing a chip pad (14) over a substrate (11);
- providing a re-distributed line (RDL) pattern (16) on the chip pad;
- providing an insulating layer (18) covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material (2, 65+); and
- providing a stud bump (20) on the portion of the RDL pattern not covered by the insulating layer.

Claim 33 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Higgins, III, US Patent 6,294,405 (hereafter Higgins).

Higgins (Figure 1) teaches a method of making a wafer-level chip scale package, comprising:

- providing a packaged semiconductor device (10) containing a chip pad (14) over a substrate (11), a re-distributed line (RDL) pattern (16) on the chip pad, an insulating layer (18) covering a portion of the RDL pattern with the insulating layer comprising a non-polymeric dielectric material (2, 65+), and then providing a stud bump (20) on the portion of the RDL pattern not covered by the insulating layer; and
- mounting the packaged semiconductor device on a circuit board (50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III, US Patent 6,294,405, as applied to claim 20 above, and further in view of Chakravorty, US Patent 6,350,668.

Higgins fails to teach the method further comprising providing a solder ball on the stud bump.

Chakravorty (figure 8d) teaches the use of a solder ball (313) on a solder stud (311).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the ball on the stud of Chakravorty in the invention of Higgins because both methods are known equivalent techniques used to attach chips to other substrates.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Claims 25 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III, US Patent 6,294,405, as applied to claim 24 above, and further in view of Chakravorty, US Patent 6,350,668.

Regarding claim 25, Higgins fails to teach the method further comprising providing a solder ball on the stud bump.

Chakravorty (figure 8d) teaches the use of a solder ball (313) on a solder stud (311).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the ball on the stud of Chakravorty in the invention of Higgins because both methods are known equivalent techniques used to attach chips to other substrates.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16

USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claims 29 and 30, Higgins fails to teach forming the stud bump by electroplating or by wire bonding (claims 29), wherein the stud bump is formed by wire bonding a Pd coated copper wire to the RDL pattern using a capillary (claim 30).

Chakravorty teaches the solder stud (311) can be formed using a wire bonder (9, 16+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the wire bonder of Chakravorty in the invention of Higgins because wire bonding is a known equivalent technique used to deposit metals.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950)).

Though Chakravorty fails to teach the use of a Pd coated copper wire, it would have been obvious to use a Pd coated copper wire because it is a conventionally known in the art material used to form stud bumps.

The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 31, the stud bump being coined shaped is an obvious matter of design choice. Design choices and changes of size and shape are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

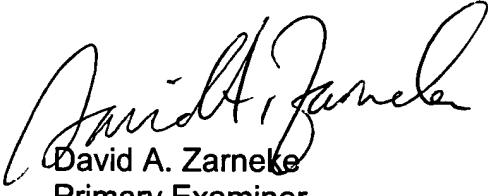
The examiner wishes to point out that Chakravorty, US Patent 6,350,668, can also be used as a 102(e) reference against at least the independent claims.

Further Wang et al., US Patent 6,362,087 (see 9, 25+ & 5, 66+), and Kim et al., US Patent 6,417,089 (see figure 4B, reference # 62), also can be used as 102(e) references against at least the independent claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (571)-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David A. Zarneske
Primary Examiner
August 28, 2004